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The input to the synthesis phase is the design, and the output consists of a design netlist that feeds into the implementation tool. The key learning from this chapter include the synthesis design process, use of tools, synthesized output files and a tutorial which describes on how to perform a synthesis.

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VHDL 101 - From Logic Gates to Adders. VHDL is all about creating logic. As a descriptive language, all the HDL languages bring something unique to programming - making true parallel logic circuit. As we take baby steps into VHDL, we will start Part 3 by looking at logic and working through to adding circuits.

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